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Behavioral DS3 Generator and Analyzer Data Sheet

Generator Features

- VHDL/Verilog component generates DS3 data. Supports Unchannelized, M23 Multiplex, and DS3 C-bit Parity Applications.
- Supports 5 types of Payload - AIS, Idle, PRBS15, Fixed Pattern, and Data from a File.
- Supports Physical Layer Convergence Protocol (PLCP) over DS3 format.
- Completely configurable via a command language and command interprettor.
- Ability to generate errors on a frame and sub-frame basis on any of the overhead bits.
- Ability to transmit any 16-bit data sequence over the C-bit channel.
- Stuff under command control on a per-frame basis.
- Generate dump and log files.
- Complies with ANSI T1.107-1995.

Generator Entity Description

```
ENTITY ds3_generator IS
  Generic(
  Cmd_File_Name    : string;  -- command file
  Dump_File_Name   : string;  -- binary data file
  Log_File_Name    : string;  -- formatted data
  Payload_File_In  : string   -- optional payload file
  );
  Port (
  clk              : IN std_logic:   --clock
  resetn           : IN std_logic;   -- reset
  data_out         : OUT std_logic;-- serial data out
  frame_sync       : OUT std_logic;-- X1 bit
  sub_frame_sync: OUT std_logic-- sub-frame
  );
END ds3_generator;
```

Analyzer Features

- Supporting analyzer will monitor DS3 data.
- Built-in framer will frame on DS3 signals or on an external frame sync signal.
- Detects 5 types of Payload - AIS, Idle, PRBS15, Fixed Pattern, and Data from a File.
- Ability to ignore frames to account for data delay through the device.
- Recognizes errors in all overhead bits.
- Completely configurable via a command language and command interprettor.
- Recognizes Stuff bits.
- Generates dump and log files.
- Complies with ANSI T1.107-1995.

Analyzer Entity Description

```
ENTITY ds3_analyzer is
  Generic(
  Cmd_File_Name    : string;  -- command file
  Dump_File_Name   : string;  -- binary data file
  Log_File_Name    : string;  -- formatted data
  Payload_File_In  : string   -- optional payload file
  Frame_Delay      : integer := 0 -- delay the frame sync
from the generator to account for device delay.
  );
  Port (
  clk              : IN std_logic;     -- clock
  resetn           : IN std_logic;     -- reset
  data_in          : IN std_logic;     -- serial data in.
  frame_sync       : IN std_logic;     -- frame sync in.
  );
END ds3_analyzer;
```


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GENERAL

The DS3 traffic generator is a programmable non-synthesiszeable VHDL/Verilog component that generates ANSI T1.107-1995 compliant DS3 frames. The applications supported are 1) M23 Multiplex Application (7 DS2 channels), 2) Unchannelized Application, and 3) DS3 C-bit Parity Application (28 DS1 channels), 4) Physical Layer Convergence Protocol (PLCP).

The DS3 generator supports five payload types - Alarm Indication Signal (AIS), Idle Signal, Pseudo-random Sequence (PRBS15 polynomial), Fixed Pattern Sequence (16-bit pattern), and Data From a File.

The DS3 generator has a built-in command interprettor and is configurable via commands from a file. Thus, it is not necessary to re-compile the VHDL/Verilog to change the behavior of the generator.

The typical way to use the generator is to specify a type of Payload (AIS, Idle Signal, Pseudo-random data, Fixed Pattern) and any Error conditions (E.g. F bits in error) followed by a Transmit (TRN) command. A command file may contain several TRN commands preceded by any of the payload or error commands.

The DS3 traffic analyzer is a programmable non-synthesiszeable VHDL/Verilog component that verifies DS3 data against ANSI T1.107-1995. The DS3 analyzer supports the same types of payloads as the generator. The type of payload is specified in a command file or the expected payload can be read from a file. The PRBS checker is self synchronizing to the received data. The analyzer detects and reports AIS and IDLE frames automatically.

There are two typical ways to use the analyzer -

One, if the expected payload is not known, the DS3 analyzer will report if the traffic received complies with ANSI T1.107-1995. In this case the payload is not checked.

Second, if the expected payload is known it can be specified in a command file and then the incoming received payload is also compared with the expected payload.

M23 Multiplex Application

This application provides 7 DS2 channels which are sequentially bit-interleaved to form the DS3 signal. The payload and overhead bits of each DS2 can be independently controlled. The “stf” command is used to send a stuff bit or a DS2 bit. This is done on a per-DS2 basis. Simultaneous errors can be created in a DS3 overhead bit or on an individual DS2 overhead bit. All this is controlled by a command language.

Unchannelized Application

This application provides framed but unchannelized DS3 signals. The DS3 application preserves the M, F, P, X, and C-bits. All C-bit commands are available as described in the DS3 C-bit Parity Application.

DS3 C-bit Parity Application

The DS3 C-bit parity application preserves the M, F, P, X, and C-bits as defined in the standard. This application uses a 2-step multiplex process. First, 7 DS2s signals are created. Each of these are built of 4 DS1 signals. The DS1 signals are unframed clear channel. All 7 stuff time slots in the DS3 frame will be stuffed.

PLCP Application

The PLCP command specifies that the payload in the DS3 frame complies with the PLCP standard. Commands can be issued to control the PLCP overhead bytes, or set errors on them.The stuff command is used to control the trailer lenght.

Command Summary

Cmd Name	Description
#	Comment Character
-	Comment Character
*	Comment Character
dev	Specify the Device type
mod	Select the Application
ign	Ignore Frames
dmp	Dump enable
dis	Display on/off
ais	AIS
idl	Idle
pns	Pn-sequence
pat	Fixed Pattern
fil	Data from a file
trn	Transmit
set	Set PLCP overhead bytes.
flip	Set errors on PCLP overhead bytes.
stf	Stuff DS3
err	Error on overhead bits
cbt	C bit control

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