TENESIX INC.

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Low Latency Image Processing Pipeline in a Xilinx or Altera FPGA

Tenesix has developed an FPGA-based Low-Latency Image Processing Pipeline. Available in both Xilinx and Altera families, the Pipeline is customized to suit many applications including Medical Imaging, Endoscopy, Surveillance, Stereoscopy, Infra Red Imaging and 3-D Sensing.

Sensor Calibration and Correction:
First-order correction (gain and offset, or two-point correction) is applied to incoming pixel data to account for variations in temperature or differences among sensors elements. A state-less area ordering filter is used to suppress the effects of defective pixels.

Demosaic:
Several demosaicing algorithms are available to interpolate a complete image from partial raw data received from a color-filtered image sensor using a Color Filter Array (CFA).

Display Pre-Calibration (Gamma Correction, Smoothing & Sharpening):
Sometimes due to the physical characteristics of the materials used, the response of image sensors to light at different wavelengths does not match in color and linearity the human visual system. A 3x3 matrix is used to manipulate and correct the color representation of the sensor. Gamma correction, a nonlinear operation to code and decode luminance or tristimulus values is used to linearize the response curve of both the sensor and the display systems. A sharpening filter is used to pre-correct for the modulation-transfer-function (MTF) of the display and the Contrast Sensitivity Function (CSF) of the user. These filters pre-correct the nonlinear behavior of the displays.

Display Pipeline (Output Synchronization, Size Adjustment, Interlacing, Overlays & Output Formatting):
The display pipeline synchronizes the sensor to the display rate using external DDR2/3 memory. If the sensor size does not match the display size, the image is resized to place the image anywhere in the display. Several resizing algorithms are available. The image is interlaced and overlays inserted before formatting the output to match the display (DVI, VGA, S-Video, Composite).

Noise Reduction and Contrast Enhancement:
Two histogram equalization circuits with region of interest, gain limits and dual-peak controls are available. Sensor noise is minimized by a single-pole IIR filter or a Gaussian filter. A median filter with different masks is available to reduce salt and pepper noise.

Customer Algorithms:
The above blocks calibrate and correct the sensor, pre-calibrate the display, and display the image on a monitor. Customer specific algorithms are inserted in between the sensor pipeline and the display pipeline. These include programmable filters, fixed and adaptive thresholding algorithms, and binary filters (Dilation, Erosion, Closing, Opening, Rank). Dewarping algorithms are used to map an image from an input space to an arbitrary geometric output space. Auto focus, stereo image synchronization, motion detection and image stabilization algorithms can be added to the pipeline.

All pipelines are customized to minimize latency and FPGA size

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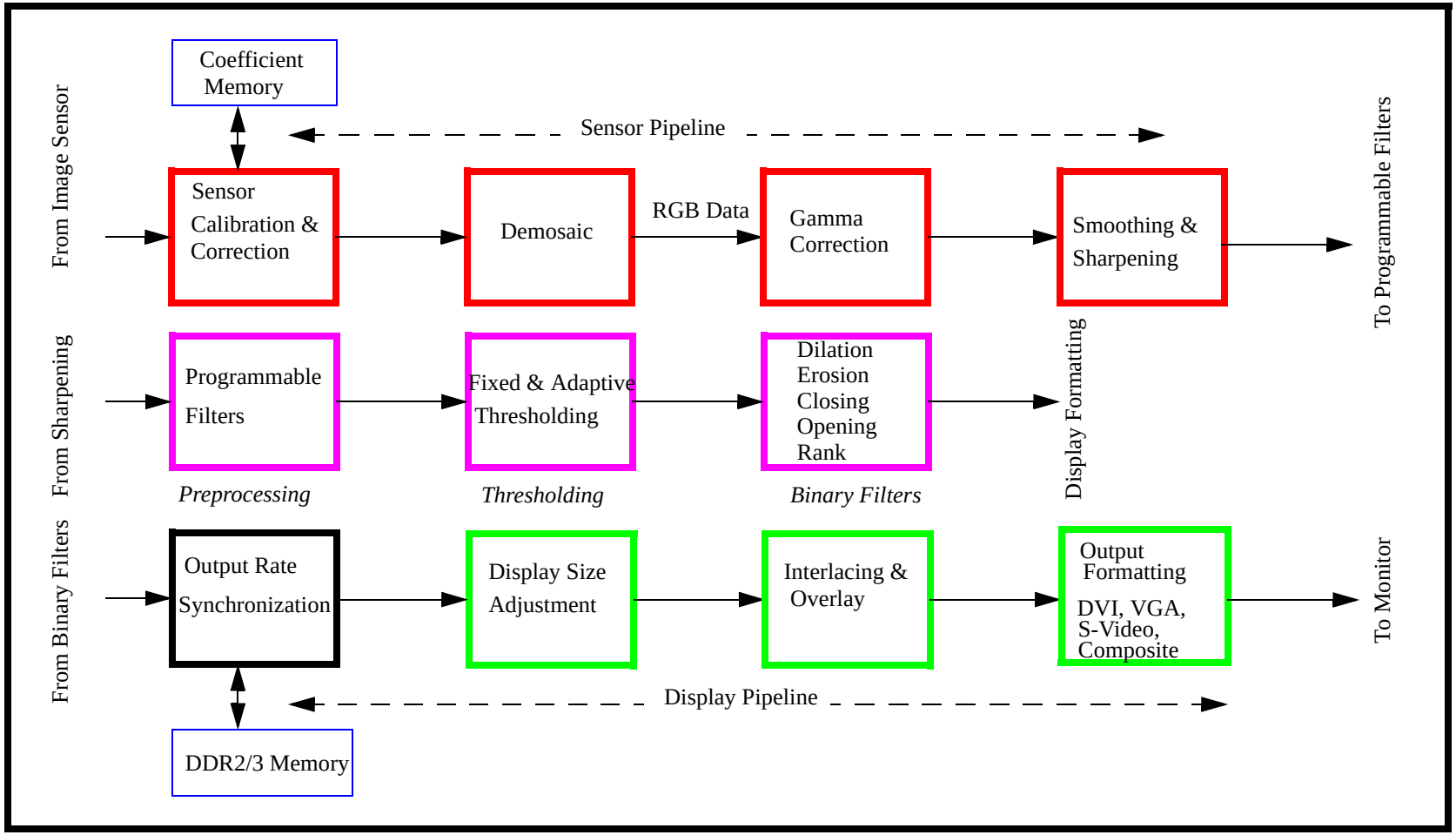
Fig 1: FPGA-Based Low-latency Image Processing Pipeline



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