TENESIX INC.

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Intel IXF1002 “Verilog” Verification Component

The IXF 1002 Verification Component is a package of **Verilog** files for integration within a “**Verilog**” verification environment. The IXF1002 Verification Component is used to inject an Ethernet MAC formatted data into a Device Under Test (DUT) or to monitor an Ethernet MAC formatted data from a DUT. The payload within the Ethernet frame is either a fixed pattern, an incrementing pattern or Pseudo Random Binary sequence.
The Verilog Model complies with the Intel IXF1002 Dual port Gigabit Ethernet Controller, May 2001 specification.

IXBUS BFM Object

- The component suite uses one active port with a programmable ID number.
- Models the Ready signal at the RX interface.
- The bus-functional models supports a programmable FIFO threshold to model the TX interface.
- Supports internal loopback.

Scheduler Object

- The scheduler provides data on RX side based on a credit based round robin scheduling algorithm.
- The scheduler supports bandwidths with a 64 Kbps granularity with programmable de-rating factor.
- Uses a comprehensive map based configuration for bandwidths and de-rating factor.

Frame Demux Object

- This object decodes the destination address field on the incoming frame and sends it to MAC monitors.
- Supports both VLAN and MPLS mode of operation.

MAC Generator / Monitor

- Supports IEEE 802.3z Gigabit Ethernet frame standard and IEEE 802.1Q Virtual Bridged Local Area Networks(VLAN) standard.
- Supports upto 16384 programmable channels configurable as VLAN or MPLS.
- Packet length is programmable and can be random on a per-channel basis.
- Select between 32-bit CRC or no CRC.
- Specify fixed or random interval betweeen packets with CRC errors.
- Model the arrival of error-free packets with either a Normal, Poisson or Uniform Distribution.

Payload Generator / Monitor

- Generate/Verify payload for the MAC Generator/Monitor.
- Insert/Verify header in the payload for in-band verification.
- Insert/Verify unique source address in the in-band header.
- Insert/Verify packet sequence number in the in-band header.
- Monitor for dropped packets/cells on a channel using the sequence numbers in the in-band verification header.
- Specify a fixed pattern, incrementing sequence or pseudo random sequence on a per channel basis.
- Generate a PASS/FAIL indication on a per-channel basis.
- Selected channel is sent to the transcript in debug mode.
- Generator/Monitor report on bandwidth transmitted/received.

Contact Tenesix at 978 244 9074 or email to sales@tenesix.com

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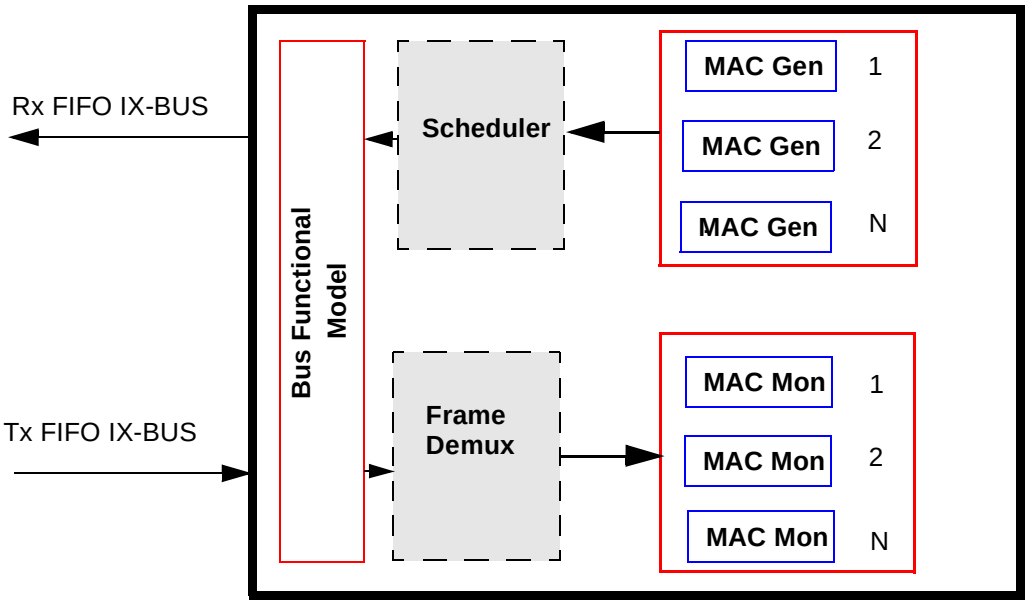

Fig 1 : Intel 1002 Verification Component