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SPI-3 Link Layer "e" Verification Component

*The SPI-3 "**e**" Verification Component (SPI-3 eVC) is a package of E files for integration with an "**e**" verification environment. The SPI-3 eVC emulates the Link Layer Device in both the ingress and egress directions and is used to connect to a Multi-Port Physical Layer (PHY) Device Under Test (DUT).*

The SPI-3 eVC is used to inject ATM Cells or Packet (payload only) data into a SPI-3 PHY DUT and to monitor ATM Cells or Packet data from a SPI-3 PHY DUT. Each channel on a PHY can be configured to carry either ATM cells or Packet data.

SPI-3 eVC Environment

- The tester may configure the number of PHY devices under test. Currently, only 1 PHY is supported.

SPI-3 Injector

- One SPI-3 injector per PHY.
- User configurable number of channels per PHY (up to 256).
- Individually configure channels, each channel may carry different types of data.
- User configurable transfer size in bits (8 or 32).
- User configurable polling address bus size in bits.
- User configurable transfer burst size specified in Packets, Cells or Cycles . The injector transmits bursts a programmable number of packets or cells on selected channel before switching the transmission source to another channel.
- User configurable "pause" behavior. Ability to control pause via the TENB signal. Ability to specify Packet, Cell or Cycle based interval for transition to pause mode. The pause duration is specified in number of cycles.
- User configured "post FIFO full" transmit duration in cycles. The injector interface will continue to transmit data for this number of cycles after the PHY DUT has indicated near FIFO full condition on a channel with DTPA, STPA or PTPA signals.This feature may be used to overflow the PHY's FIFOs. For ATM traffic, transmission will continue to the end of the cell that is currently being transmitted (on selected channel).
- Polling of channels for Transmit Packet Available status with DTPA, STPA or PTPA signals.
- Insert parity errors on a channel basis, specified as a percentage of total test time.
- Insert packet errors via TERR signal on a channel basis, specified as a percentage of total test time.

SPI-3 Collector

- One SPI-3 collector per PHY.
- User configured number of channels per PHY (up to 256).
- Configure expected behaviour of each channel, each channel may carry different types of data.
- Interface to PHY DUT is SPI-3 compliant.
- User configured transfer size in bits (8 or 32).
- User configured "pause" behavior. Ability to control pause via the RENB signal. Ability to specify Packet, Cell or Cycle based interval for transition to pause mode. Ability to specify duration of pause in number of cycles.
- Ability to turn on/off parity verification.
- Monitor ADDR, SOP, EOP sequence to detect PHY errors.
- Enable/disable pass through of erroneous packets. If pass through is enabled, packets indicated by the PHY as being in error (with RERR signal) will be passed to the Packet Monitor for analysis. If pass through is disabled, erroneous packets are discarded.
- Ability to customize levels of error reporting.

Contact Tenesix at 978 244 9074 or email to sales@tenesix.com

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ATM Cell Generator / Monitor

- Generate/verify ATM Cells as requested by the SPI-3 injector.
- Generate/verify user configurable VPI, VCI, GFC, CLP, PTI and HEC fields.
- Optionally scramble/descramble (X**43) payload.
- Insert a user specified number of bit errors in the HEC field.
- Optionally corrupt a user specified percentage of ATM Cells with a variable number of HEC errors.

Packet Generator / Monitor

- Generate/verify packet data (payload only) as requested by the SPI-3 injector.
- Optionally scramble/descramble (X**43) payload.

Payload Generator / Monitor

- Generate/verify payload data for the ATM Cell or Packet generator.
- Insert/verify header in the payload for in-band verification.
- Insert/verify destination address for payload - user specified the destination address for each channel.
- Insert/verify unique source address (channel number) in in-band header - source address is the channel number.
- Insert/verify packet sequence number in in-band header.
- Generate/verify information bits - user can specify source of information bits as a fixed pattern or incrementing sequence.

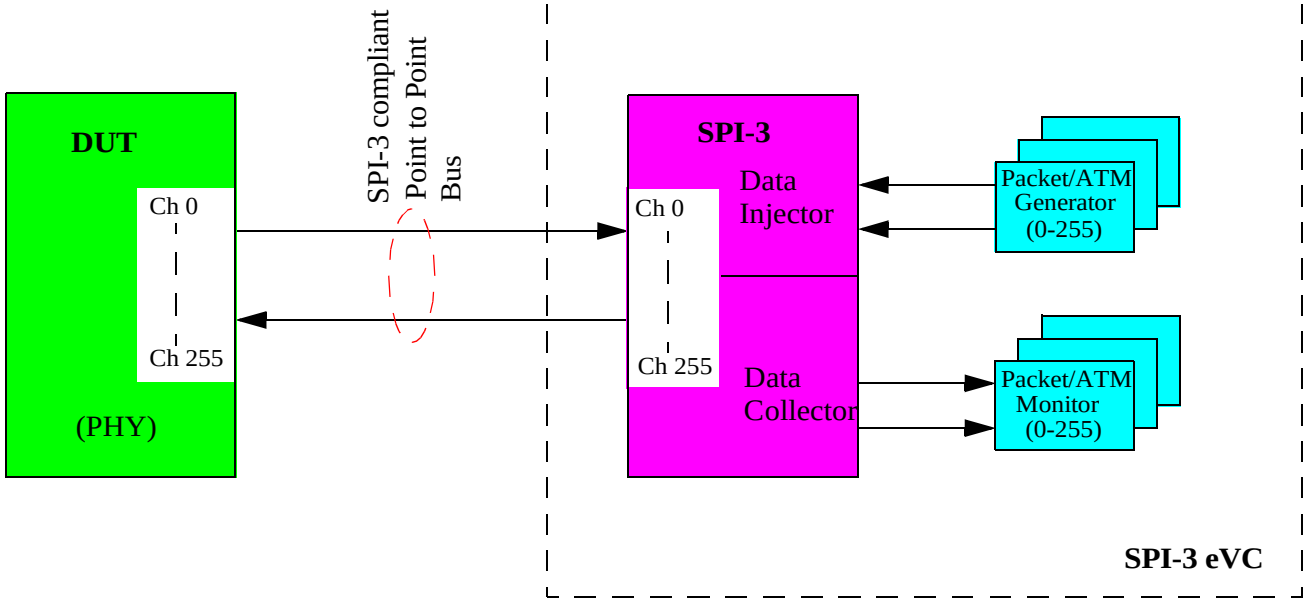

Figure 1 : Link Layer SPI-3 eVC Interface to SPI-3 Compliant Device Under Test (DUT)