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SPI-3 PHY Layer “e” Verification Component

*The SPI-3 PHY Layer “**e**” Verification Component (SPI-3 eVC) is a package of E files for integration with an “**e**” verification environment. The SPI-3 eVC emulates the Physical Layer Device in both the ingress and egress directions and is used to connect to a Multi-Port Link Layer Device Under Test (DUT).*

The SPI-3 eVC is used to inject ATM Cells or Packet (payload only) data into a SPI-3 Link Layer DUT and to monitor ATM Cells or Packet data from a SPI-3 Link Layer DUT. Each channel on the eVC can be configured to carry either ATM cells or Packet data.

SPI-3 eVC Environment

- The tester may configure the number of Link Layer DUT’s. Currently, only 1 DUT is supported.

SPI-3 Injector

- One SPI-3 Injector per Link Layer DUT.
- User configured number of channels per Link Layer DUT (up to 256).
- Ability to individually configure channels, each channel may carry different types of data.
- User configured transfer size in bits (8 or 32).
- User configured polling address bus size in bits.
- User configured transfer burst size specified in Packets, Cells or Cycles. The transmit interface bursts a programmable number of packets or cells on a particular channel before switching the transmission source to another channel.
- User configured “pause” behavior by controlling the RVAL signal level. Ability to specify Packet, Cell or Cycle based interval for transition to pause mode. The pause duration is specified in number of cycles.
- User configurable FIFO FULL behavior. Ability to control FIFO FULL via the DPTA, STPA or PTPA signals. Ability to specify Packet, Cell or Cycle based interval for transition to FIFO FULL mode. Ability to specify duration in number of cycles of FIFO FULL mode.
- Ability to insert parity errors on a channel basis, specified as a percentage of total test time.
- Ability to insert packet errors via RERR signal on a channel basis, specified as errors per number of packets.

SPI-3 Collector

- One SPI-3 Collector per Link Layer DUT.
- User configured number of channels per Link Layer DUT (up to 256).
- Ability to configure expected behavior of individual channels, each channel may carry different type of data.
- User configured transfer size in bits (8 or 32).
- Ability to control number of bytes accepted after FIFO FULL.
- Ability to turn on/off parity verification.
- Monitoring of ADDR, SOP and EOP sequence to detect Link errors.
- Ability to enable/disable pass through of erroneous packets. If pass through is enabled, packets indicated by the Link Layer as being in error (with TERR signal) will be passed to the Packet Monitor for analysis. If pass through is disabled, erroneous packets are discarded.
- Ability to customize levels of error reporting.

ATM Cell Generator / Monitor

- Generate/verify ATM Cells as requested by the SPI-3 injector.
- Generate/verify user configurable VPI, VCI, GFC, CLP, PTI and HEC fields.
- Optionally scramble/descramble (X**43) payload.
- Insert a user specified number of bit errors in the HEC field.
- Optionally corrupt a user specified percentage of ATM Cells with a variable number of HEC errors.

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Packet Generator / Monitor

- Generate/verify packet data (payload only) as requested by the SPI-3 injector.
- Optionally scramble/descramble (X**43) payload.

Payload Generator / Monitor

- Generate/verify payload data for the ATM Cell or Packet generator.
- Insert/verify header in the payload for in-band verification.
- Insert/verify destination address for payload - user specified the destination address for each channel.
- Insert/verify unique source address (channel number) in in-band header - source address is the channel number.
- Insert/verify packet sequence number in in-band header.
- Generate/verify information bits - user can specify source of information bits as a fixed pattern or incrementing sequence.

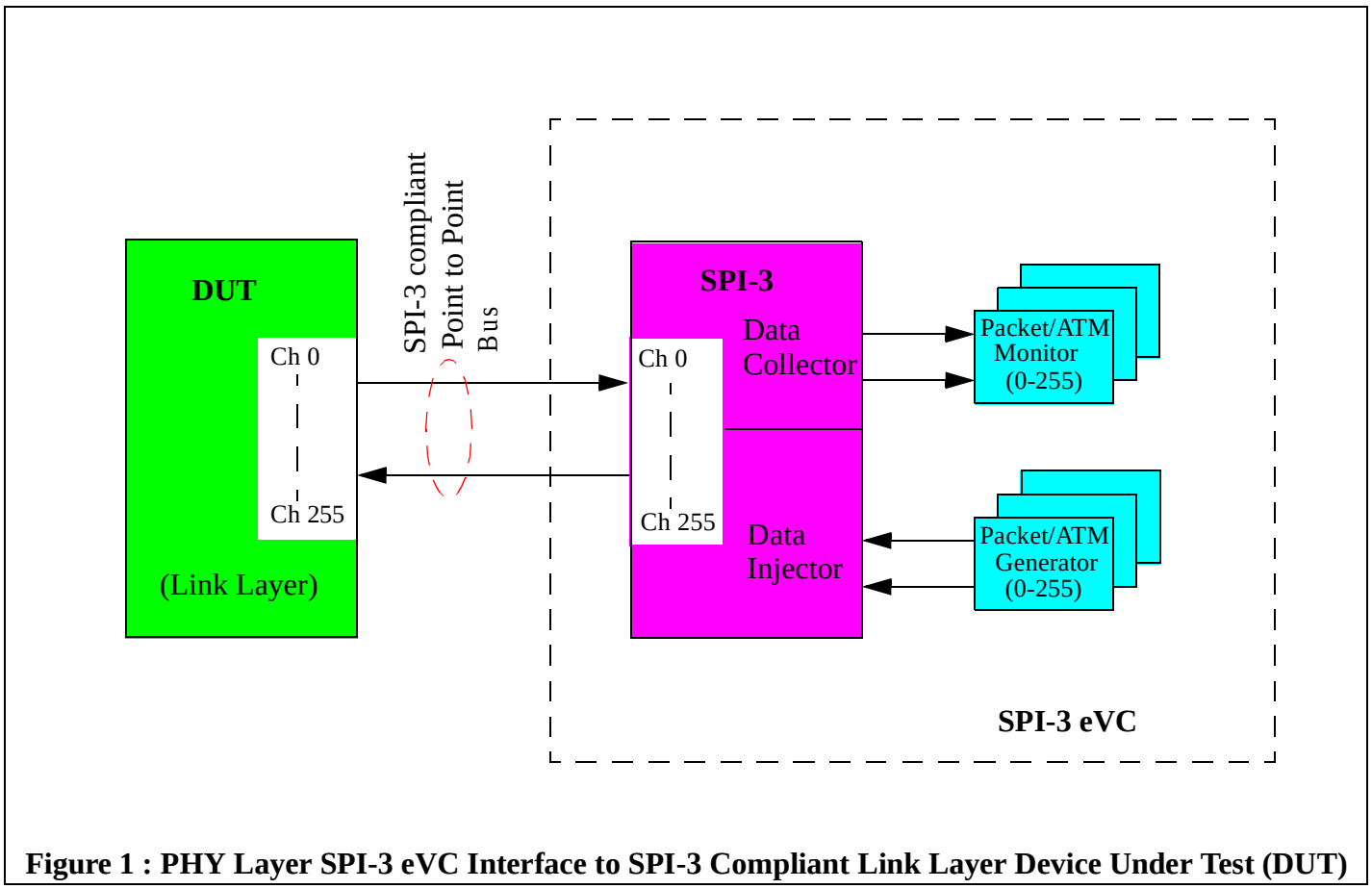

Figure 1 : PHY Layer SPI-3 eVC Interface to SPI-3 Compliant Link Layer Device Under Test (DUT)