TENESIX INC.

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Vitesse VSC 9675 “Verilog” Verification Component

The Vitesse VSC 9675 Verification Component (VC) is a package of object-oriented **Verilog** files for integration within a “**Verilog**” verification environment. The Vitesse 9675 VC is used to inject a clear channel DS3 or TDMe formatted data into a Device Under Test (DUT) or to monitor a clear channel DS3 or TDMe formatted data from a DUT. The payload within the DS3/TDMe frame is Bit Sync HDLC encapsulated PPP data (RFC 1662). The Verification Component provides an abstract level of program control for up to 672 HDLC encapsulated PPP channels per DS3 and hides the lower level implementation of the protocol. The bandwidth for each PPP channels is programmable with a DS0 granularity and support for Multi-Link PPP (RFC 1990) is provided.
The Verilog Model complies with Vitesse VCS 9675 Scalable Architecture Framing Engine with M13, Databook Draft Revision 1.0d Specification.

Port Configuration

- Number of independent DS3 ports is programmable. Each port has a programmable ID.
- Specify number of channels configured.
- Specify the bandwidth of a channel with a DS0 granularity.
- Specify a channel to be of type PPP or Multi-Link PPP.
- Bus-functional model supports posedge and negedge clear channel DS3 with clock gapping.
- Supports Robbed-bit signalling.
- In TDMe mode, the DS1 TDMe Sync and the DS3 TDMe Sync45 pulse can be offset under program control.
- Supports a loopback mode for the verification component to operate in **self-checking** loopback.

HDLC Generator/Monitor

- Supports Bit-Sync Mode as defined in RFC 1662 and ISO/IEC 3309.
- Supports up to 672 programmable channels per DS3.
- Select/Verify the intergap fill to be a byte or a bit.
- Specify fixed or random number of back-to-back (without an intergap fill) packets.
- Model the arrival of back-to-back packets with either a Normal, Poisson or Uniform Distribution.
- Specify duration of the intergap fill as fixed or random within a specified range.
- Model the duration of the intergap fill with either a Normal, Poisson or Uniform Distribution.

PPP Generator/Monitor

- Generate/Verify PPP packets on a demand basis.
- Supports up to 672 programmable channels per DS3.
- Generate/Verify ADDRESS, CONTROL, PROTOCOL, DATA, CRC fields.
- Select between 32-bit CRC, 16bit CRC-CCITT, 16 bit CRC or no CRC.
- Specify fixed or random interval betweeen packets with CRC errors.
- Model the arrival of error-free packets with either a Normal, Poisson or Uniform Distribution.
- Packet length is programmable and can be random on a per-channel basis.

Payload Generator/Monitor

- Generate/Verify payload for the PPP Generator/Monitor.
- Insert/Verify header in the payload for in-band verification.
- Insert/Verify unique source address in the in-band header.
- Insert/Verify packet sequence number in the in-band header.
- Monitor for dropped packets/cells on a channel using the sequence numbers in the in-band verification header.
- Specify a fixed pattern, incrementing sequence or pseudo random sequence on a per channel basis.
- Generate a PASS/FAIL indication on a per-channel basis.
- Selected channel is sent to the transcript in debug mode.
- Generator/Monitor report on bandwidth transmitted/received.

Contact Tenesix at 978 244 9074 or email to sales@tenesix.com

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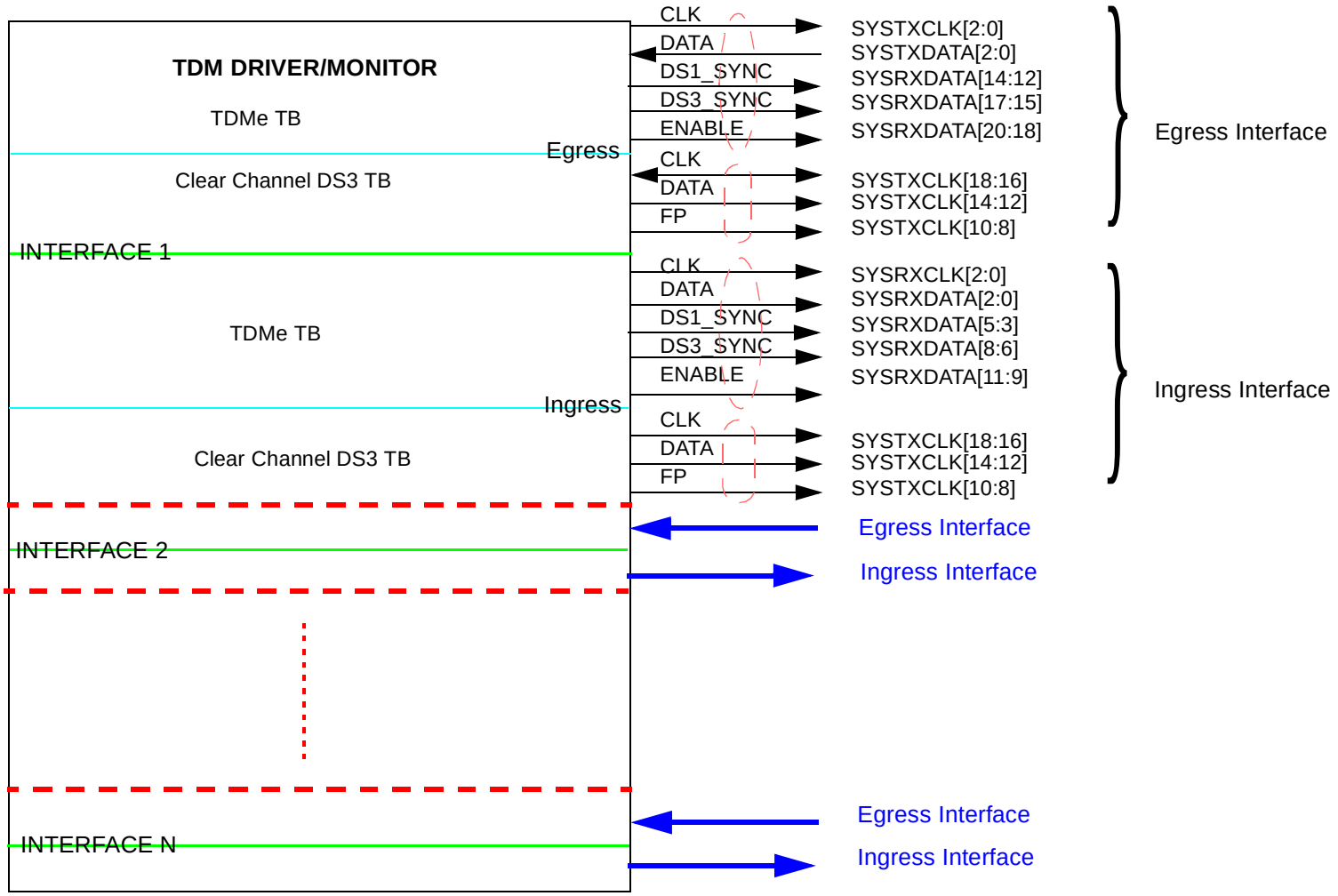

Fig 1: Vitesse VSC 9675 Verification Component