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Infrared Scene-based Autofocus Core

Product Brief
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Features

- Simple Parallel bus with FSYNC, LSYNC, Clock and Data interface to an external sensor
- Parametrized pixel depth up to 16 bits
- Supports sensors up to 4 M Pixels
- Frame rates up to 60 Frames per second
- Sensor clock rate up to 125 MHz
- Includes a noise reducing filter
- Programmable algorithm selection
- SPI interface to a microprocessor
- Provides a focus metric every frame
- External memory not required
- Optional position encoder counters
- Customized for individual applications

Applications

The Infrared Scene-based Autofocus Core can be used as part of any Infrared application that requires a motor to control the focus. Typical applications include Infrared Cameras and Microscopes. The algorithm design makes the Core especially suited for low Signal to Noise conditions.

Infrared Autofocus Core Resources	
Sample Specifications	
Supported Device	Spartan/Cyclone
Device Tested	Spartan 6
LUTS	1894
DSP48A1	4
RAMB16WER	6
DCM	1
Special Features	None
Provided with Core	
Documentation	Product Brief, Data Sheets (Device and Test Bench) and Test Suite
Design File Formats	Compiled Library, EDIF netlist, BIT File, POF File.
Constraints File	qpf/qsf files
Verification	Behavioral Simulation, Matlab, Laboratory
Instantiation Templates	VHDL
Reference	None
Additional Items	None
Simulation Tool Used	
Model Tech. ModelSim 6.0	
Support	
Provided by Tenesix Inc.	

General Description

Figure 1 below shows a block diagram of the Infrared Autofocus Pipeline. The Infrared Autofocus Pipeline accepts pixel data from a sensor via FSYNC, LSYNC, HSYNC and Data signals. The incoming data is filtered and the scene analyzed to calculate a focus metric. The focus metric is sampled and saved real-time every frame and sent to a microprocessor via a Serial Peripheral Interface (SPI). The microprocessor is used to configure the Core and can read on demand the value of the metric. The method to calculate the metric and the incoming data filter are configurable via the microprocessor. In a typical application, the microprocessor controls the motor to move the lens assembly thus generating a new metric. The search algorithm and search strategy to find the best focus position are typically implemented in the microprocessor.

The Core optionally accepts one or more sets of Quadrature Phase A, Phase B and Limit Up and Limit Down signals typically output by position encoders on the lens assembly. These signals are filtered and used to increment or decrement an Encoder Counter. The separate Encoder Counts are provided to the microprocessor via the SPI interface.

The sensor clock rate, frame rate and pixel depth are customized. Sensor frame rates up to 60 frames per second are supported. The pipeline supports sensors up to 4 MPixels with a Pixel Depth up to 16 bits and a Pixel clock rate up to 125 MHz. External memory is not required. An H-bridge interface to a motor driver chip can be added if required.

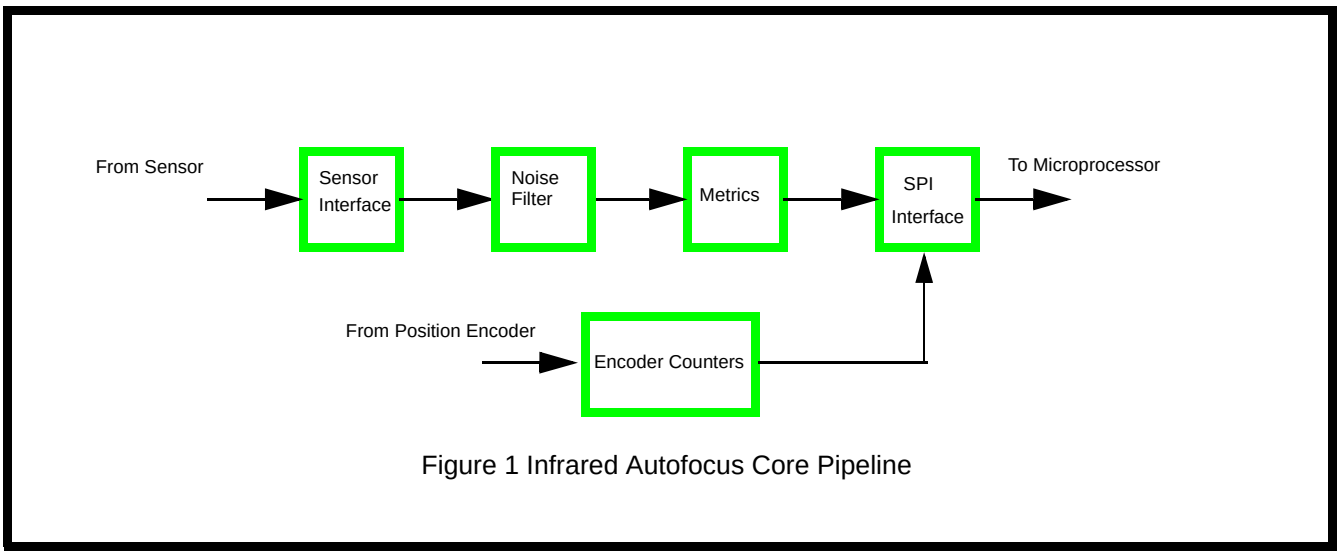

Figure 1 Infrared Autofocus Core Pipeline

Recommended Design Experience

The following experience is recommended for the user to implement the complete digital camera pipeline and to facilitate easy use of the same.

- Familiarity with the Standard Cell/FPGA architecture
- Familiarity with the tools used

Ordering and further Information

To learn more about this or any other core, contact
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