Double Data Rate (DDR)- DRAM Controller

Product Brief
January 2002

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Features

- Fully complaint to JEDEC -DDR-II specifications
- Double data rate architecture; two data transfers per clock cycles
- Bidirectional data strobe (DQS)
- DQS is edge aligned with data for reads center-aligned with data for writes
- Single DQS signal for each data byte
- Differential clock outputs
- Commands are driven on each rising clock edge
- Optional data mask for write
- Burst lengths of 2, 4 or 8
- CAS Latency 2 or 2.5
- Four banks concurrent operation
- Bank interleaved for zero dead cycles
- Internally generated activate, precharge and refresh commands
- Configurable bus width 8, 16, 32, 64 or 72
- Programmable timing parameters - RP, RRD, RCD, RFC and MRD
- Programmable refresh interval
- Programmable drive strength
- Simple memory like system interface
- Transaction queue for commands
- Streamlined ASIC/FPGA portable design
- Customized test bench for easy functional and timing verification
- Easy integration with an external MPU device/code
- All the inputs are registered before use
- All the outputs are driven directly from the Q output of a Flip-Flop
- Programmable edge select on memory read data
- Can be easily extended to a future JEDEC standard
- Seamless interface to Micron DDR-SDRAMs
- Proven on Stratix FPGA

Applications

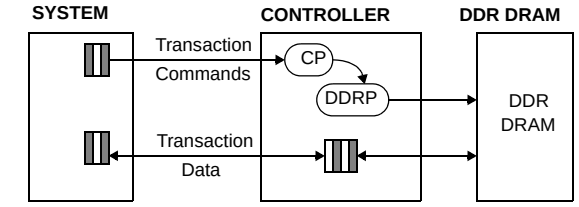
The DDR DRAM controller can be used as part of any application that requires an external DRAM. Typical applications include processors, video graphics and network devices.

DDR-DRAM Controller Tip Facts	
Specifications	
Supported Device	Virtex II/Stratix/ASIC
Device Tested	Stratix
Logic Cells	803
Registers	516
Performance	133MHz
Tools	NA
Special Features	None
Provided with Core	
Documentation	Product Brief, Data Sheets (Device and Test Bench) and Test Suite
Design File Formats	Compiled Library, EDIF netlist, BIT File, POF File.
Constraints File	ucf/xcf/dc shell files
Verification	Fully automated behavioral verilog/VHDL
Instantiation Templates	VHDL, Verilog
Reference	JEDEC, Micron
Additional Items	None
Simulation Tool Used	
Model Tech. ModelSim 5.5e	
Support	
Provided by Tenesix Inc.	

General Description

The DDR-DRAM controller accepts transaction commands from the user logic and performs these commands on the external DDR-DRAM. It internally generates activate, command (read/write) and precharge commands according to the transaction size and burst length. It also generates the auto-refresh commands as required by the DDR-DRAM.

The controller can be parameterized to suit the required use. A typical application of the DDR-DRAM controller is shown in Figure 1.



CP: Transaction Command Processor
DDRP: DDR Command Processor.

Figure 1. DDR DRAM controller application

The controller can interleave subsequent commands (if accessing different banks) so that there are zero dead cycles between commands.

The controller has the following programmable counters that are accessible via the micro processor.

Parameter	Description
Burst length	The number of data words that are transferred between the DRAM and the transaction data queue on each read/write command. Allowed values are 4 or 8.
CAS latency	The number of clock cycles to wait for after a read command to the memory and receiving the data. Typical values are 2 or 2.5.
Drive Strength	External DDR-DRAM pad drive strength, as specified for the DRAM.
Precharge command period (RP)	Is the number of clock cycles that must elapse between a precharge command and bank becoming accessible for the next command. Supported range is 0 ~ 15.
Activate command period (RRD)	Is the number of clock cycles that must elapse between two activate requests (on different banks). Supported range is 0 ~ 15.

Table 1: Programmable timing parameters

Parameter	Description
Activate to read/write (RCD)	Is the number of clock cycles that must elapse between an activate command and a read/write command on the same bank. Supported range is 0 ~ 15.
Auto-refresh command period (RFC)	Is the number of clock cycles that must elapse between an auto refresh command and any further access on the dram. Supported range is 0 ~ 15.
Write Recovery (WR)	Is the number of cycles to wait after the last write command and precharging the same bank. Supported range is 0 ~ 15.
Load mode register command period (MRD)	Is the period of a load mode register command. The controller waits for these many clock cycles after a load mode register command. Range is 0 ~ 15.
RD-WR Turn Around Cycles (RWC)	Is the number of clock cycles for read-write bus turn around. Supported range is 0 ~ 15.
Auto-refresh command timer	Is the number of clock cycles that must elapse between two refresh commands. The controller issues a refresh command every time this counter expires. Supported range is 0 ~ 65535.
DRAM DLL initialization timer	Is the initialization time for the DLL to be stable inside the dram. The controller accesses the dram after this counter is expired. Supported range is 0 ~ 65535.

Table 1: Programmable timing parameters

All the timing parameters are programmed as an integer number of clock cycles. That is for a 100MHz clock, interfacing to a memory whose RCD requirement is 75ns, the programmed RCD value has to be 8 (nearest high value). A programmed value of zero, indicates that the next command can follow immediately. In the above example, if RCD is less than 10ns, RCD can be programmed to be zero.