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Low Latency Color Camera Pipeline Core

Product Brief
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Features

- Simple Camera Link interface to an external sensor
- Parametrized pixel depth up to 16 bits
- Color Filter Array Interpolation (Demosaicing) with parametrized Bayer Pattern
- Supports sensors and displays up to 4 M Pixels
- Sensor and Display Frame Rate from 0 - 60 Fps
- Sensor and display clock rate up to 125 MHz
- Drives an NTSC or PAL display
- Supports DVI, VGA, S Video and Composite Video
- Directly connects to an external NTSC/PAL driver
- Supports True Interlaced, Pseudo Interlaced and Progressive Scan
- Programmable Recursive Filter
- Color Balance in RGB or Bayer Space
- Median Filter in RGB or Bayer Space
- Several median filter masks supported
- Histogram Equalization in RGB or Bayer Space
- Programable Histogram parameters
- Gamma Correction
- Frame buffer to synchronize the Sensor Pipeline to the Display Pipeline
- External memory interface up to 250 MHz
- Frame buffer interfaces to external SRAM
- Parameterized number of frames of storage
- Minimize latency with as little as 1 frame of storage
- Arbitrary relationship between sensor and display frame formats
- Easy integration with an external microprocessor
- All the inputs are registered before use
- All the outputs are driven directly from the Q output of a Flip-Flop
- Customized for individual applications

Applications

The Digital Camera Pipeline can be used as part of any application that requires an external sensor to display an image on an NTSC or PAL monitor. It is especially suited for low-light, low-latency applications and can be customized for individual applications. Typical applications include Medical Imaging, Endoscopy, Surveillance and 3-D Sensing.

Color Camera Pipeline Resources	
Sample Specifications	
Supported Device	Cyclone/Stratix/ASIC
Device Tested	Stratix
Logic Elements	7124
Multipliers (18 x 18)	10
RAM M512	4
RAM M4K	58
Special Features	None
Provided with Core	
Documentation	Product Brief, Data Sheets (Device and Test Bench) and Test Suite
Design File Formats	Compiled Library, EDIF netlist, BIT File, POF File.
Constraints File	qpf/qsf files
Verification	Behavioral Simulation, Matlab, Laboratory
Instantiation Templates	VHDL
Reference	External Memory Data Sheet
Additional Items	None
Simulation Tool Used	
Model Tech. ModelSim 6.0	
Support	
Provided by Tenesix Inc.	

General Description

Figure 1 below shows a block diagram of the Digital Color Camera Pipeline. The Digital Camera Pipeline accepts pixel Bayer Data from a sensor and outputs RGB Data to an external NTSC/PAL Driver which connects to an NTSC/PAL monitor. This core consists of two pipelines. The first pipeline is the Sensor pipeline used to interface to the sensor and contains those filters operating in Bayer Space. The other pipeline is the NTSC/PAL display pipeline. The NTSC/PAL pipeline drives RGB Data to an external NTSC/PAL driver chip and contains those filters operating in Color Space. The display pipeline is synchronized to the sensor pipeline at the Frame Buffer which interfaces to external SRAM.

The sensor clock rate, frame rate and pixel depth are customized. Sensor frame rates of 0 - 60 frames per second are supported. The pipeline supports sensors up to 4 MPixels with a Pixel Depth up to 16 bits and a Pixel rate up to 125 MHz. The display pipeline can run at a display rate up to 125 MHz. The external memory interface runs up to 250 MHz.

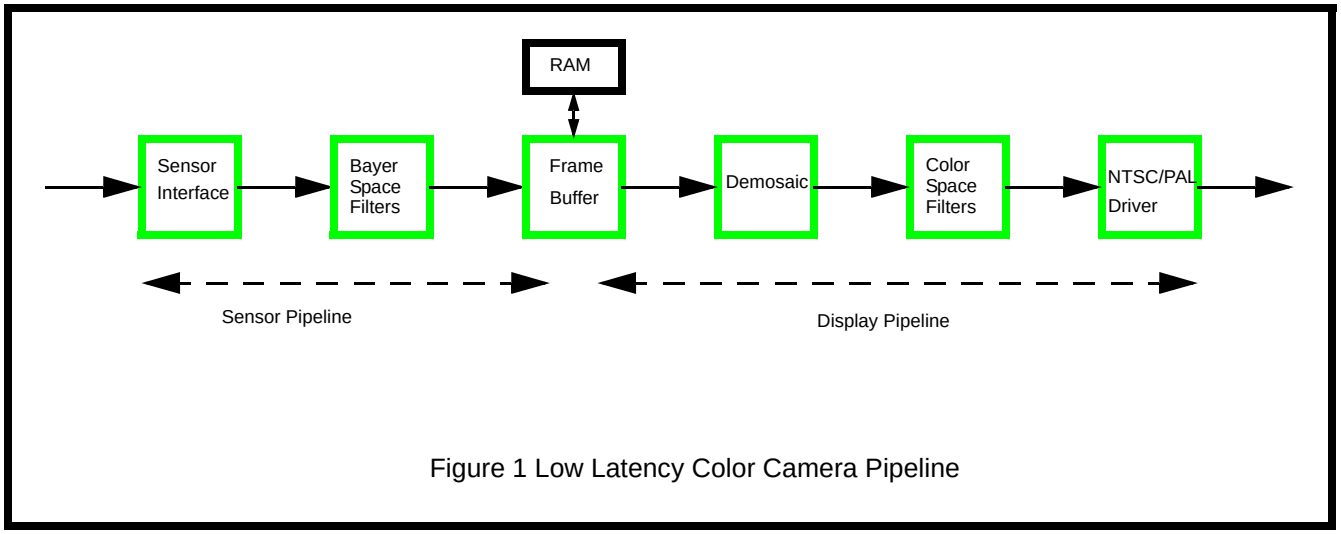

Figure 1 Low Latency Color Camera Pipeline

Recommended Design Experience

The following experience is recommended for the user to implement the complete digital camera pipeline and to facilitate easy use of the same.

- Familiarity with the Standard Cell/FPGA architecture
- Familiarity with the tools used
- Understanding of SRAM standards/data sheets.

Ordering and further Information

To learn more about this or any other core, contact

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