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Tip™

Infiniband Link Layer Core 10 - 80 Gbps

Product Brief
January, 2007

Features

- Fully Complaint with IB 1.2 Specification
- Available at 10 Gbps, 20 Gbps, 40 Gbps or 80 Gbps
- Available with 1x, 4x or 8x Physical Lanes
- Available with 1, 2, 4, 8 or 15 Virtual Lanes
- Very Low Latency
- CRC Generation and Checking
- Link Layer Flow Control
- Shadow Buffer for Preemptive Updating of Credits
- Programmable Flow Control Period
- Protocol Error and Packet Length Checking
- Simple 64 bit or 128 bit FIFO interface
- Interfaces to an Internal or External SERDES
- Fully Synchronous Design
- Single 125 MHz, 250 MHz or 500 MHz Clock
- Streamlined ASIC/FPGA portable design
- Proven design, shipping in FPGAs and ASICs
- Tested in the lab with Mellanox Switches
- Delivered with Test Bench and Test Cases
- Delivered in the Altera Stratix or Xilinx Virtex family

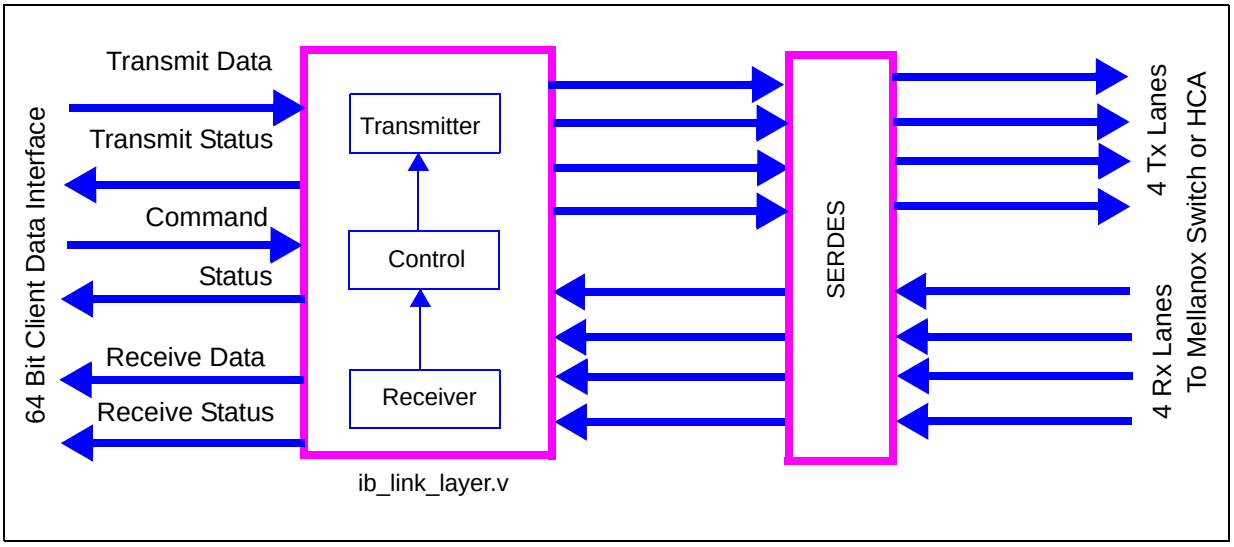

Figure 1 Four Physical Lane Example

Applications

The IBXDR family of Infinband Link Layer Cores is typically used in Target Channel Adapters and in Bridges. Customers have used this core to bridge a variety of protocols to Infiniband. Some examples of protocols being bridged to Infiniband are PCI, 1G or 10G Ethernet, Hypertransport, SPI4, and Fiber Channel. Another application for the IBXDR is in high-speed high-bit rate data gathering for video or radar data acquisition.

General Description

The IBXDR is a family of Infiniband (IB) Link Layer Cores which are typically used in a Target Channel Adapter (TCA) or for High-speed Data Acquisition. They connect through an internal or external SERDES to an IB Switch or directly to a Host Channel Adapter. On the parallel side they connect to the Client Interface via a simple FIFO-like bus.

The IBXDR Core can be ordered with 1, 2, 4, 8 or 15 Virtual Lanes. Each core always has Virtual Lane 15 for sub-net management. The customer can select 1X, 4X, or 8X number of Physical Lanes. The IBXDR Family of Cores supports 10Gbps, 20 Gbps, 40 Gbps or 80 Gbps. The 40 Gbps and 80 Gbps cores are available only as an ASIC core while the 10 Gbps and 20 Gbps cores are available as FPGA or ASIC cores. Both Xilinx and Altera FPGAs are supported.

In the Transmit Direction, the core checks for errors, segments the packets, appends the ICRC and VCRC and sends the data out to the SERDES. The status of each packet is reported on the Transmit Status Interface.

In the Receive Direction, the core checks the ICRC and VCRC, checks for packet errors and sends the packets along with the status to the Client Interface. Packet by packet status is available on the Receive Status Interface.

The IBXDR Core has a simple Command Interface to set the internal state machines. All other controls are via a pin interface i.e. there are no programmable registers. All status is available at the pins.

The Client Receive Buffers are queried every cycle and when necessary, Flow Control Packets are automatically generated. The core maintains a shadow register which predicts if the other side is running low on credits and preemptive flow control packets are sent to keep the throughput at the maximum. The minimum flow control period is programmable.

The design is a cut-through design and depending on the core results in only 2 - 4 clock cycles of latency.

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Ordering and Further Information

To learn more about this or any other Tip cores, contact

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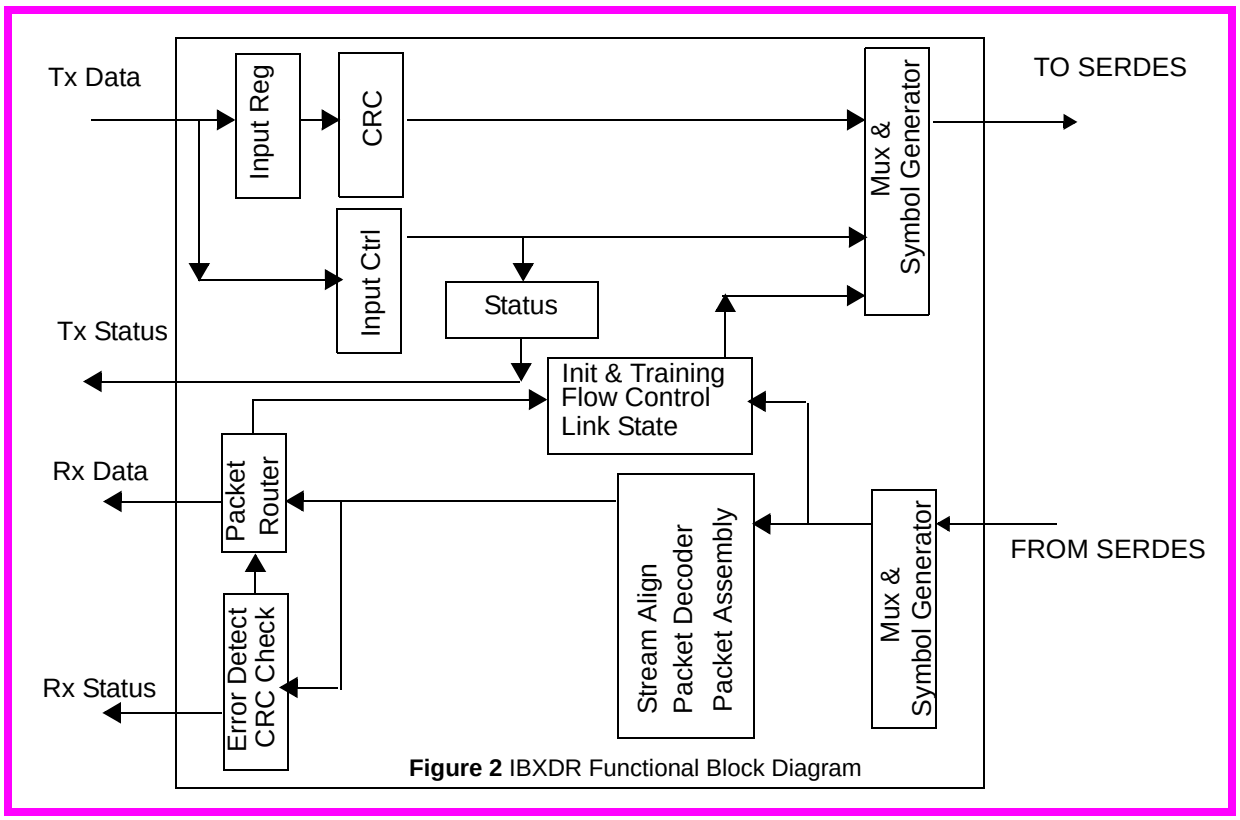

Figure 2 IBXDR Functional Block Diagram