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Tip™

Infiniband Transport Layer Core 10 - 20 Gbps

Product Brief
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Features

- Fully Complaint with IB 1.2 Specification
- Interfaces seamlessly with IB Single and Double Data Rate Link Layer Core
- Unreliable and Reliable Options available
- UC Send and UC RDMA Write
- RC Send, RC RDMA Write and RC RDMA Read
- Supports 1024 Queue Pairs
- Programmable Queue Pair Control Block
- 2 GByte messages
- End-to-end Flow Control
- 511 Reliable Requests in Flight
- Auto Acks and RNR is supported
- Simple 64 bit DMA interface
- Uses external DDR2 RAM for Retry Memory
- Fully Synchronous Design
- Single 125 MHz Clock
- Streamlined ASIC/FPGA portable design
- Proven design, shipping in FPGAs
- Tested in the lab with Mellanox Switches
- Delivered with Test Bench and Test Cases
- Delivered in the Altera Stratix or Xilinx Virtex family

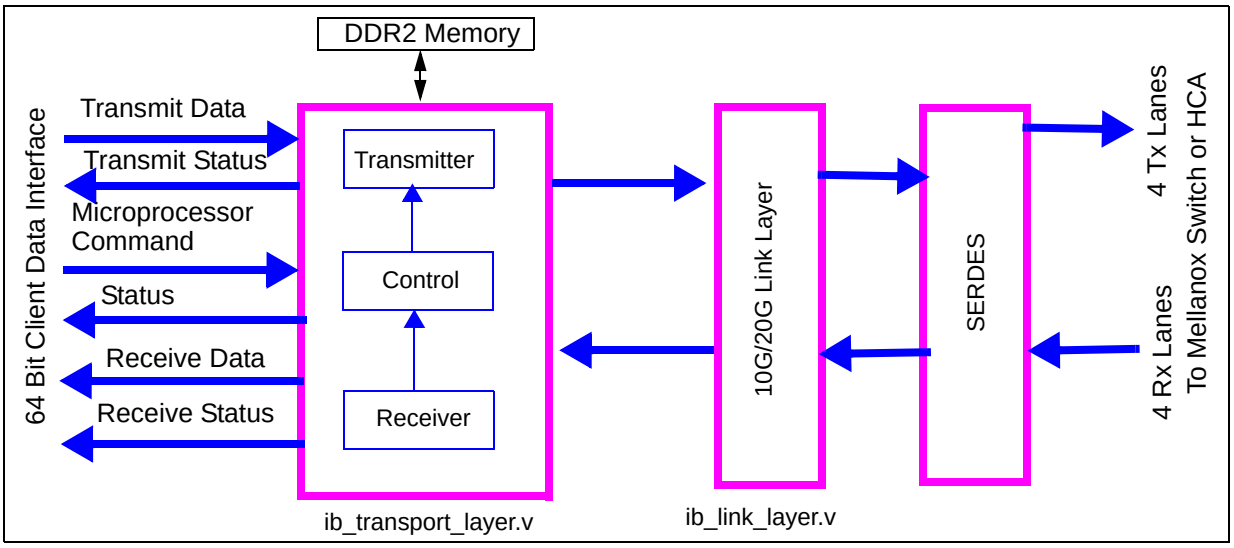

Figure 1 Typical Target Channel Adapter

Applications

The IBXTR family of Infinband Transport Layer Cores is typically used in Target Channel Adapters and in Bridges. Customers have used this core to bridge a variety of protocols to Infiniband. Some examples of protocols being bridged to Infiniband are PCI, 1G or 10G Ethernet, Hypertransport, SPI4, and Fiber Channel. Another application for the IBXTR is in high-speed high-bit rate data gathering for video or radar data acquisition.

General Description

The IBXTR is a family of Infiniband (IB) Transport Layer Cores which are typically used in a Target Channel Adapter (TCA) or for High-speed Data Acquisition. They connect through a companion IB Link Layer Core to an internal or external SERDES which is connected to an

IB Switch or directly to a Host Channel Adapter. On the Client side is a parallel DMA bus to get data in and out of the Transport Layer Core.

The IBXDR Core can be ordered as a UC (Unreliable Connect) Core only or as a RC (Reliable Connect) Core. The UC Core is used mainly for data equitation applications. The RC Core supports both RC and UC functions. Both Xilinx and Altera FPGAs are supported.

In the Transmit Direction, the client sends data on any configured Queue Pair (QP) along with the QP Number, and the Service Type (E.g. Read Request or Read Response). The Core checks for errors looks up the configuration for that Queue Pair and sends the data to the Link Layer Core. The data is also stored in external DDR memory until a valid ACK packet is received. If a retry is required, the data is sent from DDR memory without the client being involved. End-to-end flow control on a message basis is maintained. The core can operate in cut-through or store-and-forward mode.

In the Receive Direction, the Core receives Data and Status from the Link Layer Core and sends it out to the Client Interface along with the QP Number, Service Type and status. When the Client acknowledges receipt of the message the Transmit Side sends out an ACK packet to acknowledge error-free reception of the data. An auto-ack mode is provided which when enabled will automatically send out an ACK packet in response to a valid request packet.

The Core provides a separate interface for Queue Pair “0” and “1”. Data on this interface is sent directly to the Link Layer Core. Thus, using this “soft” interface, the Client can send other services not supported by the Core.

The IBXTR Core has a simple CPU Interface to configure and read both the Transport and Link Layer Cores. The CPU programs the Queue Pair Control Block with Retry Counts, Response Time Out Value, Inter-Packet Delay, Service Level, Services Supported on this Queue Pair, Destination Queue Pair, Virtual Lane, P_KEY and DLID. 1024 Queue Pairs are supported.

The RC Core is available in FPGAs only while the UC Core is available for use in an ASIC or in a FPGA.

Ordering and Further Information

To learn more about this or any other Tip cores, contact

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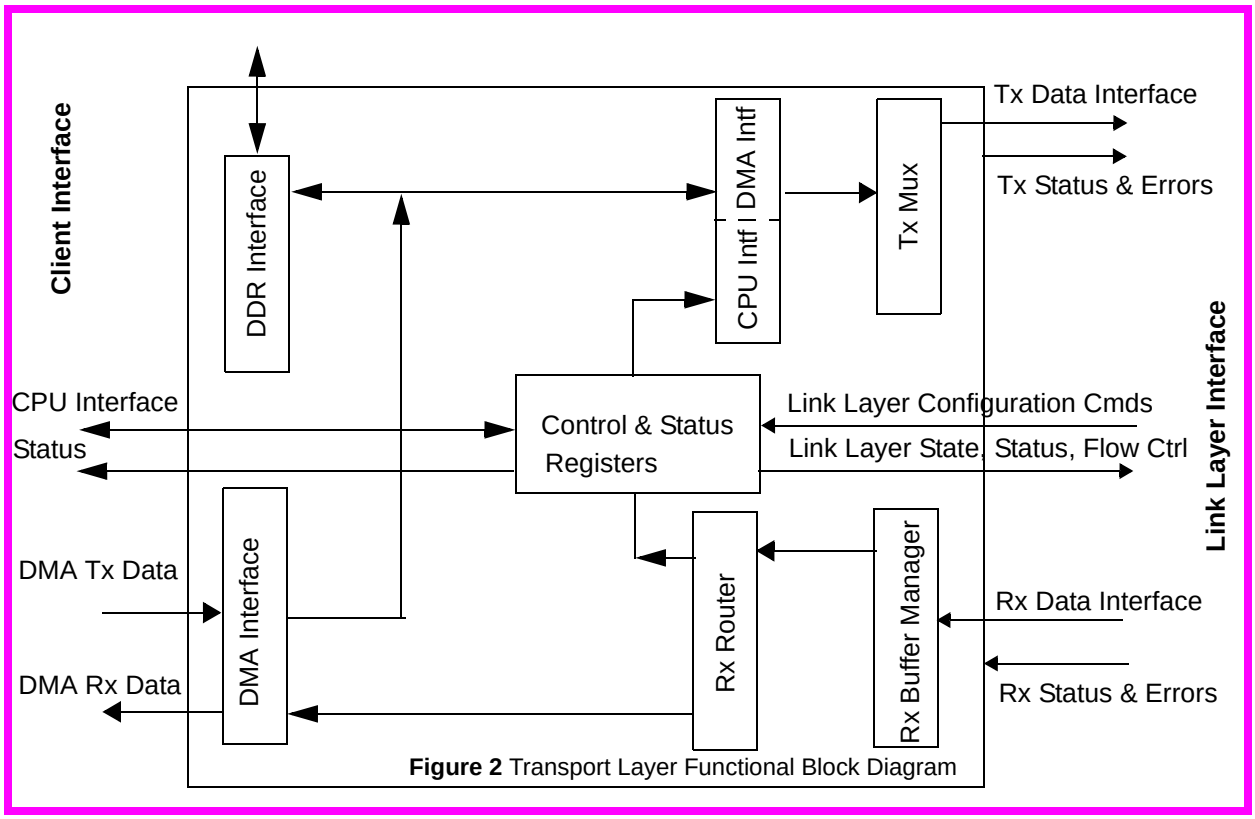

Figure 2 Transport Layer Functional Block Diagram