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Tip™

STM-16/4xSTM-4 (2.5G) TO - 48 E3 Mapper/Demapper

Product Brief
September 2003

Features

- 4xSTM-4/1xSTM-16 TU3-E3 mapper and demapper
- Complaint with ITU-G.707, SONET ANSI T1.105, and GR-253-CORE
- Asynchronous E3 mapping
- Independent 48 E3 receive and transmit channels
- Selectable add/drop of E3 channels
- Non-E3 channels are looped back
- Full STM and TU Pointer Processor
- All Line/Path overhead bytes are monitored and are regenerated
- Very small gate count
- Streamlined ASIC/FPGA portable design
- Fully synchronous design at internal 78MHz
- Can be easily upgraded to 155MHz/311MHz to reduce the gate count
- Control for external PLL for E3 jitter attenuation in the receive side
- Data/Stuff opportunity bit output indication
- Monitoring of E3 frames in the transmit direction
- Supports 16-bit asynchronous and synchronous microprocessor interface up to 78 MHz
- Mates seamlessly with TADM
- Delivered in Stratix or Virtex family

Applications

The SE3M2G5 is a versatile mapper/demapper that is used to carry 48 E3 channels in an STM-16 or 4xSTM-4 SDH/SONET streams. A typical application of SE3S2G5 as an end-user device is shown in Figure 1. Since each of the E3 channels are running independently they can be distributed for further mapping and demapping into E3 clear channel, E1 and/or D0 payloads.

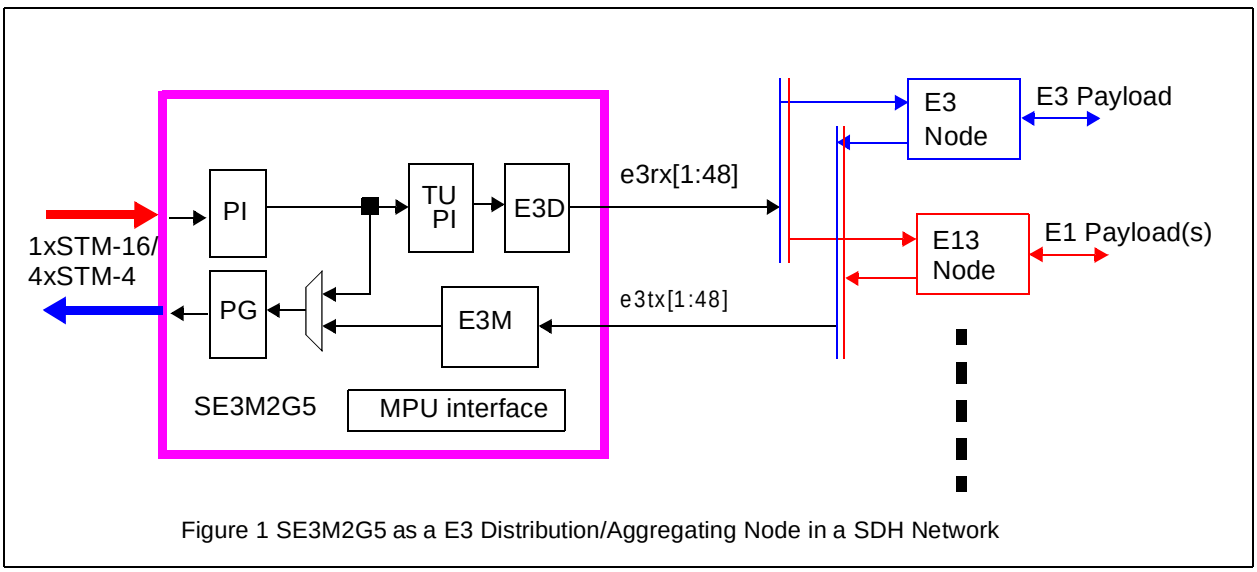

Figure 1 SE3M2G5 as a E3 Distribution/Aggregating Node in a SDH Network

General Description

The SE3M2G5 accepts 4xSTM-4/1xSTM-16 stream(s) in the line side. The data is framed and the line overhead bytes are monitored. The H1H2 bytes are processed by the pointer interpreter and the path overhead bytes are monitored. The individual STM1 SPEs are then separated into TU3s. These TU3s are then passed to the transmit side or to the TU pointer interpreter. The TU pointer interpreter then extracts the VC3 data which is passed to the E3 demapper.

The E3 demapper extracts the E3 payload from the VC3 SPEs and writes them to a bit FIFO. The C1/C2 bits are interpreted and based on majority decision used to determine whether the S1/S2 bits are data bits or stuff bits. The S1/S2 bit interpretations are also passed to an external PLL. This PLL is used to generate the 34.368MHz E3 clock from the 78MHz line clock. The S1/S2 bit indication is used for frequency adjustments.

In the transmit direction, the received E3 is written into a bit FIFO and is read and mapped into a VC3 SPE. Depending upon the average elastic store fill, the S1/S2 bits are populated in the outgoing frame with data or stuff bits. A smooth regular insertion of stuff/data bits into the S1/S2 bits is provided to reduce jitter at the far end. The TU pointers in the outgoing STM1 are set to 0x253. A functional block diagram of the SE3M2G5 is shown in Figure 2.

Ordering and further Information

To learn more about this or any other Tip cores, contact

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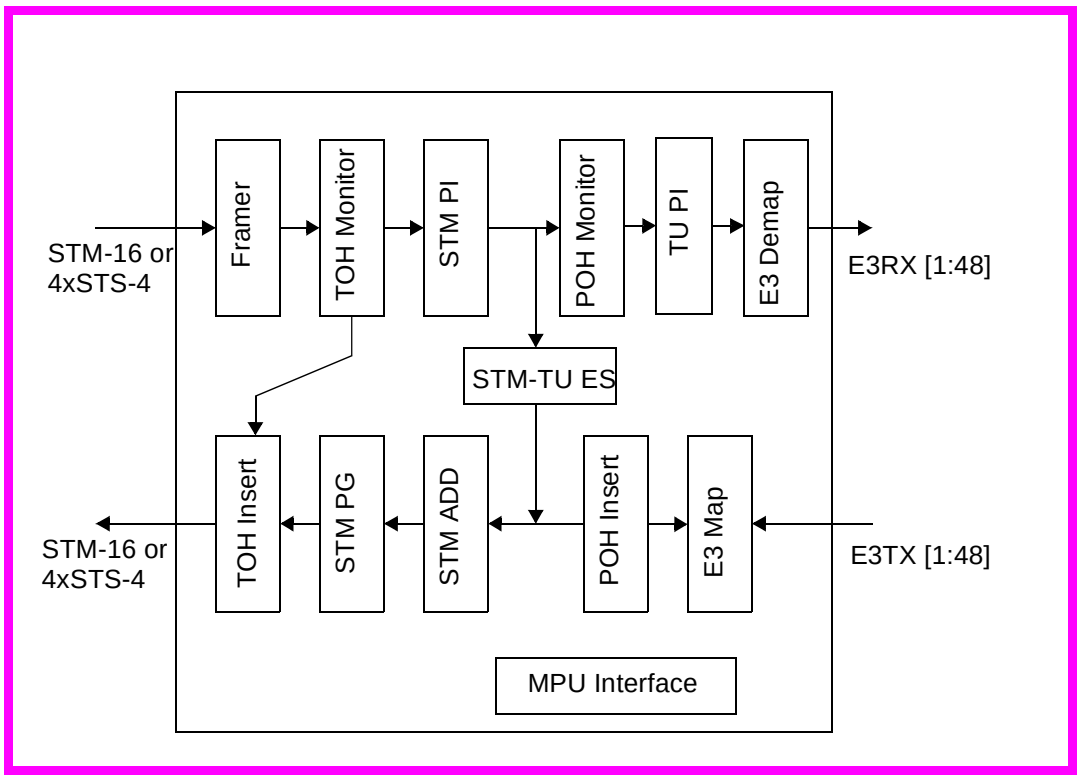

Figure 2 SE3M2G5 Functional Block Diagram