Tenesix Inc.
ASIC & FPGA Consultants for Network and Communications

20 Taylor Street
Littleton, MA 01460
Phone:+1 978 486 3749
Fax:+1 978 486 3752
URL:http://www.tenesix.com
E-mail:sales@tenesix.com

3xSTS-12/STM-4 STS/AU VT/TU Cross Connect

Product Brief
February , 2003

Features

- 3xSTS-12/STM-4 STS/AU VT/TU non blocking cross connect
- One working channel and one protection channel for each direction of the SONET/SDH ring with an additional add/drop channel
- Compliant with SONET ANSI T1.105 and GR-253-CORE
- Allows STS-1/AU-3, STS-Mc ($2 \leq M \leq 12$), STM-Mc ($3 \leq M \leq 12$) cross connect
- Pass through of C-3 mapped TU-3 time slots
- Any valid configuration of VT-1.5/TU-11, VT-2/TU-12, VT-3 or VT-6/TU-2
- Single chip UPSR regenerator
- Supports 1:1 Protection Switching
- Supports hardware/hardware-assisted UPSR switching
- Full Pointer Interprettor and Generator down to STS-1/AU-3 level
- Full VT/TU Pointer Interprettor and Generator down to VT-1.5/TU-11, VT-2/TU-12, VT-3 and VT-6/TU-2 level
- Add/drop of STS/AU or VT/TU channels
- Simple 8-bit TDM bus on the system interface at 78 MHz
- Independent Line and System Clock
- All Line overhead bytes are monitored and regenerated
- All STS/AU VT/TU POH bytes are monitored
- STS/AU POH bytes are passed through for tributaries not carrying VT/TU(s)
- STS/AU POH bytes are generated and inserted for tributaries that carry VT/TU(s)
- All VT POH bytes are passed through
- Supports 16-byte or 64-byte J0/J1 message
- Monitoring/Insertion of V5 byte
- Supports Near-end, Far-end STS1, Far-end VT, and System Loopbacks
- Supports 16-bit asynchronous and synchronous microprocessor interface up to 78 MHz
- Fully synchronous design at internal 78MHz
- Streamlined ASIC/FPGA portable design
- Can be easily upgraded to 155MHz/311MHz to reduce the gate count
- Delivered in the Stratix or Virtex family

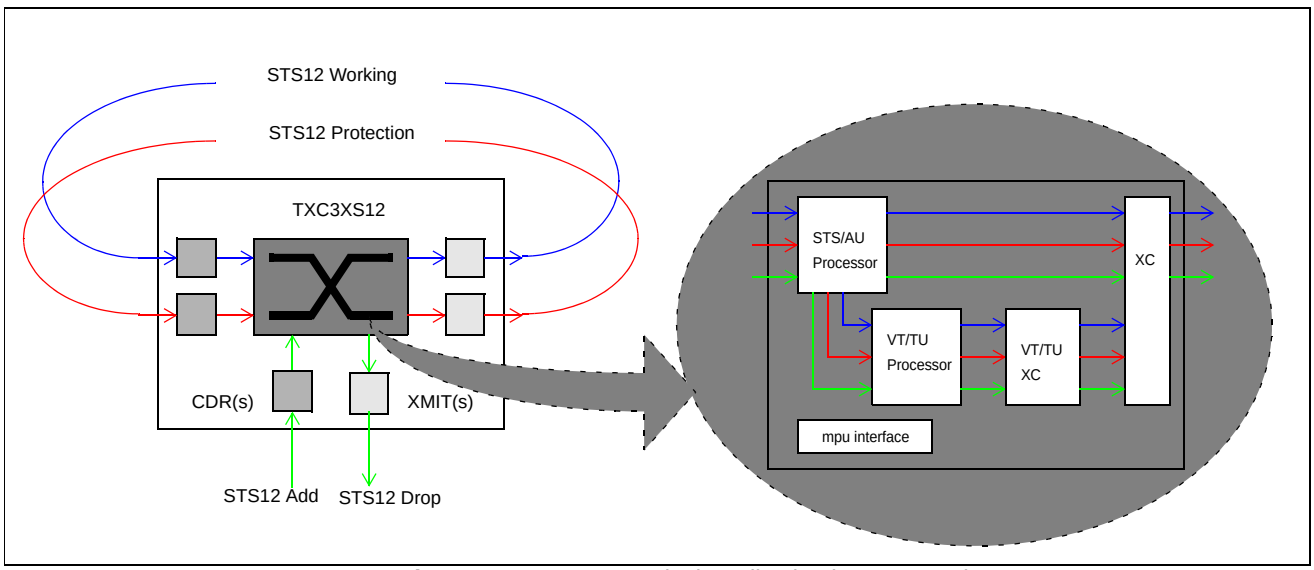

Figure 1 TXC3XS12 Typical Application in a Sonet Ring

Applications

The TXC3XS12 is a versatile cross connect that can be used as a SONET/SDH regenerator, repeater or an end user device. A typical application of the TXC3XS12 in a SONET/SDH ring as a regenerator and an add drop multiplexer is shown in Figure 1.

General Description

The TXC3XS12 accepts three STS-12/STM-4 streams. One of the streams can be from the working channel and the other one can be from the protection channel. The third stream is an optional add/drop channel. The data is framed and the line overhead bytes are monitored. The H1H2 bytes are processed by the pointer interpreter and the path overhead bytes are monitored.

The VT/TU pointer interpreter works on a VT/TU group and number basis. Thus individual groups may carry different VT/TU types. It process the V1V2 bytes and sends the data to the VT/TU cross connect.

In the transmit direction, the received STS/AU(s) or VT/TU(s) can be cross connected. The individual VTs are first cross connected, passed to the STS/AU pointer generator and then to the STS/AU level cross connect.

Both STS/AU and VT/TU cross connects support broadcast as well as multicast and are fully non blocking cross connects.

The device utilizes an UPSR switch based on hardware failure conditions to select a cross connect map which then switches the received data accordingly. Two cross connect maps are provided. One for regular switching and another one for protection switching.

If a received AU contains a TU-3 mapped C3 signal, then that time slot is allowed to pass through. Thus only time slots that carry VT data are processed by the VT cross connect.

The device supports full SDH multiplexing including but not limited to TU-3-AU3 and TU-3-AU-4 mapping.

Ordering and further Information

To learn more about this or any other Tip cores, contact

Tenesix Inc,
20 Taylor Street,
Littleton, MA 01460-1416
or visit us at www.tenesix.com
or write to info@tenesix.com

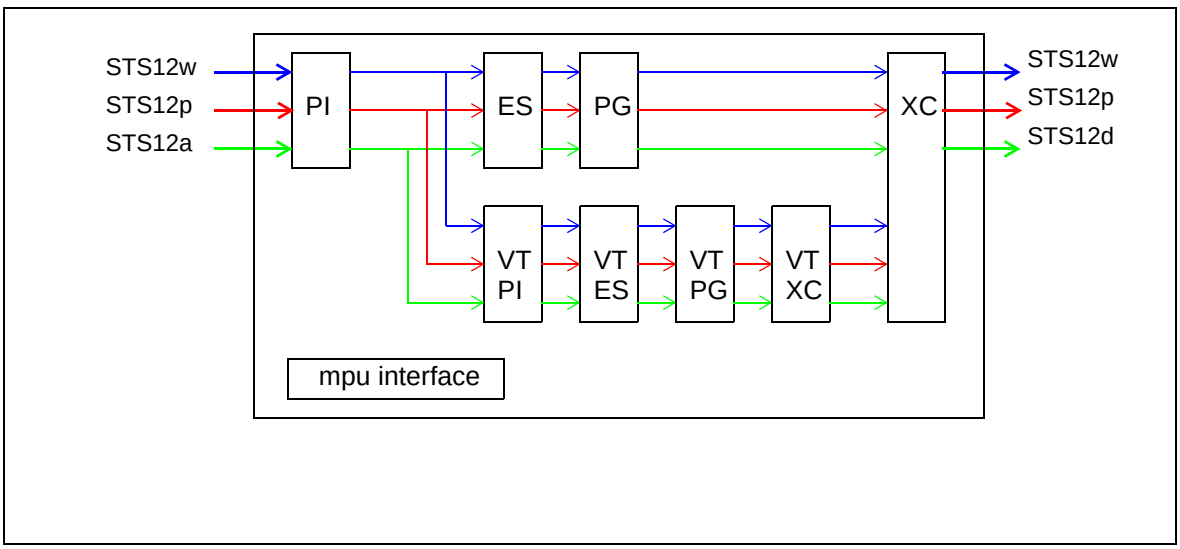

Figure 2 TXC3XS12 Functional Block Diagram