Tenesix Inc.
ASIC & FPGA Consultants for Network and Communications

20 Taylor Street
Littleton, MA 01460-1416
Phone:+1 978 486 3749
Fax:+1 978 486 3752
URL:http://www.tenesix.com
E-mail:sales@tenesix.com

Tip™

1xSTS48 - 4xSTS12 Sonet/SDH Transpose Mux/De-Mux

Product Brief
October 2003

Features

- 1xSTS-48 to 4xSTS-12 Sonet/SDH Transpose
- Four independent clocks for each STS-12
- Complaint with SONET ANSI T1.105, GR-253-CORE and ITU-T G.707
- Single FPGA mux-demux device
- Full STS Pointer Processor in Transmit Path
- B1/B2 bytes are monitored
- Generated B1/B2 bytes are optionally corrected or passed through
- Optional path performance monitoring through path overhead byte (B3) in Receive Path
- Pass through of TOH bytes
- Supports 16-bit asynchronous and synchronous microprocessor interface up to 78 MHz
- Streamlined ASIC/FPGA portable design
- Fully synchronous design at internal 78MHz
- Can be easily upgraded to 155MHz/311MHz to reduce the gate count for an ASIC
- Delivered in Stratix or Virtex family

Applications

The STP2G5 is a versatile transpose device that can be used for sonet multiplexing. It can be used as distribution node device for low order STS-12s from a STS-48.

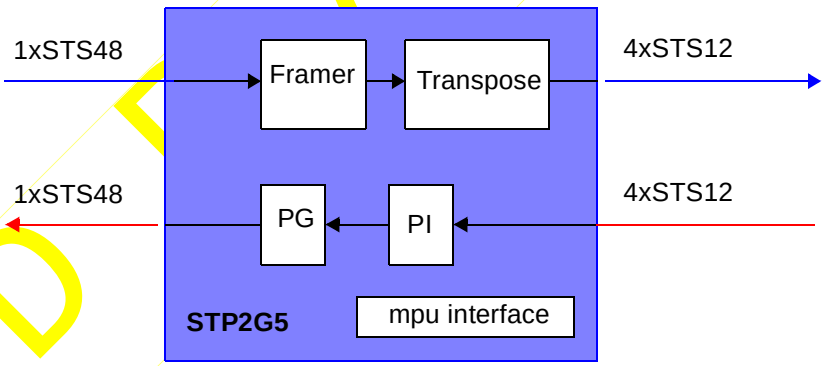

Figure 1 STP2G5 as a Tanspose Multiplexer for 4xSTS12s

General Description

The STP2G5 device accepts a single STS-48 stream and demultiplexes them to their constituent 4xSTS-12s. A functional block diagram of the STP2G5 is shown in Figure 2. On the Line side the STS-48 I/O is 32 bits wide at 78 MHz. On the System side the I/O is 8 bits wide at 78 MHz for each STS-12. A 16-bit wide microprocessor interface is used to configure and monitor the FPGA.

The incoming STS-48 is received 32 bits wide at 78 Mhz. A pseudo framer frames on the incoming data. The section and line BIP bytes are monitored (B1/B2) and a transpose demultiplexer outputs the constituent 4xSTS-12s. The section and line overhead BIP bytes are inserted in the outgoing STS-12 data streams. The other transpose overhead bytes are transparently passed through. The receive clock is sourced along with the data to ease board level routing. Each STS-12 is sent as 8-bits of data at 78 MHz.

In the transmit direction, four 8-bit wide STS-12 streams are received on four different clocks. They are independently framed and monitored for section and line BIP errors. The data is then sent to a pointer interpreter.

The H1H2 bytes are processed by the pointer interpreter and the SPE data is written into an elastic store. The B3 errors are monitored and can optionally trigger an alarm. The elastic store is read by the transmit Pointer Generator (PG) using the same frame reference for all STS-12s. Thus at the output of the PG all STS-12s are frame aligned.

A transpose multiplexer then multiplexes these STS12s into a STS48. The section and line BIP bytes are calculated and inserted. The other overhead bytes are passed through in the outgoing STS-48 stream.

Ordering and further Information

To learn more about this or any other Tip cores, contact

Tenesix Inc,
20 Taylor Street,
Littleton, MA 01460-1416
or visit us at www.tenesix.com
or write to info@tenesix.com

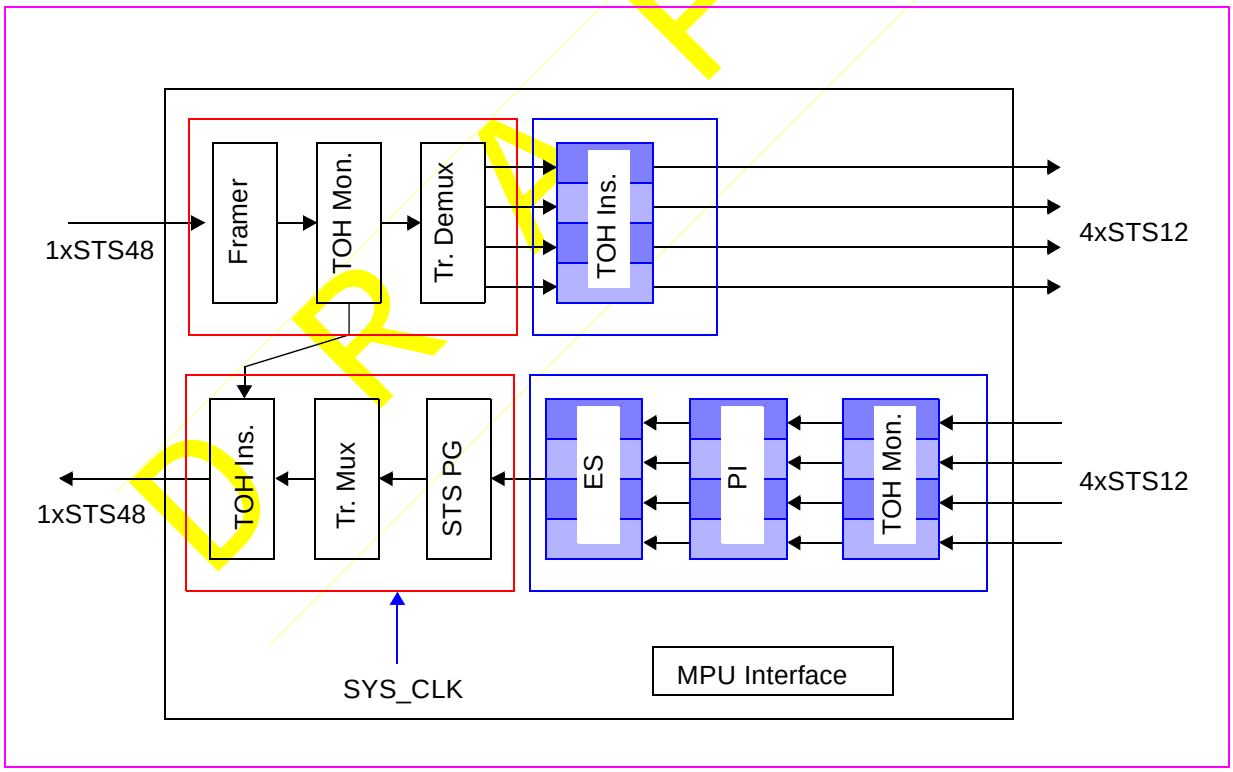

Figure 2 STP2G5 Functional Block Diagram