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ASIC & FPGA Consultants for Network and Communications

VC2G5DI

2.5Gbps STS48 VC Delay Introduction

1. Features

- Supports four STS12 622 Mbps signals operating as either 1 x STS48 or 4 x STS12
- Supports 1 to 48 STS-1 based Virtually Concatenated Groups (aggregate up to STS48 bandwidth)
- Differential delay introduction of 10 ms to 250 ms through an off-chip Double Data Rate SDRAM
- Selective pass-through for channels which are not virtually concatenated
- Synchronous/Asynchronous 16-bit address/16-bit data micro processor interface
- Input and DDR loop backs for diagnostic purposes
- Simple interface, four 8-bit data operating on a single clock
- Internal single clock of operation
- Implementation on Altera Stratix EP1S25(F780C7)
- Mates with the STM interface of a SONET device through a single-chip back plane transceiver
- Supports Dynamic Bandwidth Allocation algorithm (including LCAS inter operability in Fixed Allocation Mode)

2. Description

The VC2G5DI device introduces differential delay on Virtually Concatenated (VC) SONET traffic and forwards the data as a misaligned VC stream to a SONET device for verifying Differential Delay Compensation and Path Termination capability. This device introduces a relative network differential delay of 10 ms to 250 ms on tributaries in a STS-48 stream. An external microprocessor interface is provided to configure each STS-1 with a relative offset (delay). The device is intended to be used along with a SONET device and a back plane transceiver, or any other device supporting virtual concatenation, for verification of delay compensation functionality.

3. Applications

The device interfaces with the STM interface of a SONET device through a backplane transceiver. The incoming STM data (STS48/4xSTS12) containing Virtually Concatenated channels is first passed through a transceiver device. The back plane transceiver performs the Clock Data Recovery (CDR) function, Deserializes (Rx)/ Serializes(Tx) the data (SerDes), frames on this data and transfers it to a single system clock. The received parallel (8-bit data and 1-bit parity) data is sent to the VC2G5DI. Within the VC2G5DI, time slots are delayed relative to each other. An external DDR SDRAM is used as a delay line. Time slots which are not virtually concatenated are turned around without delay and sent back to the SONET device via the back plane transceiver. A typical application of the device is shown in Figure 1.

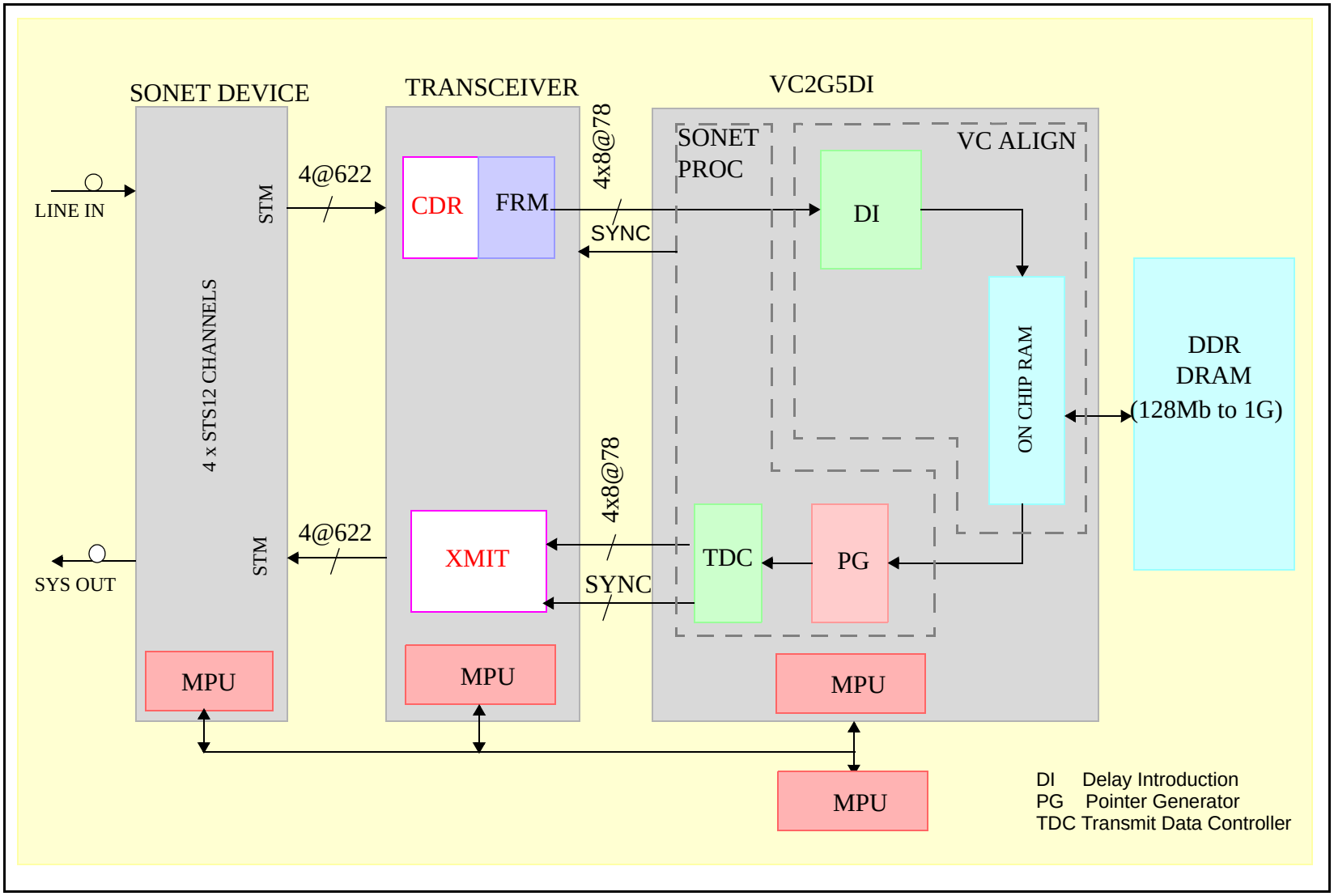

Figure 1. VC2G5DI Network Application Block Diagram